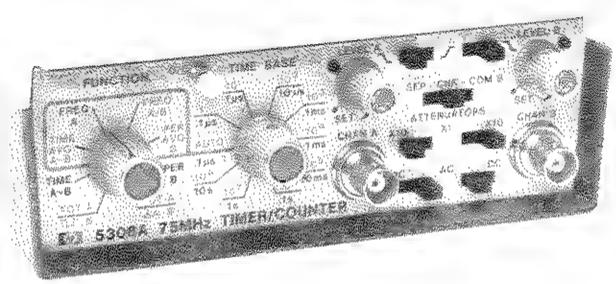
OPERATING AND SERVICE MANUAL

75 MHz TIMER/COUNTER

5308A



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CERTIFICATION

Hewlett-Packard Company certifies that this instrument met its published specifications at the time of shipment from the factory. Hewlett-Packard Company further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship for a period of one year from the date of shipment. Hewlett-Packard will, at its option, repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard, and provided the preventive maintenance procedures in this manual are followed. Repairs necessitated by misuse of the product are not covered by this warranty. NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

If this product is sold as part of a Hewlett-Packard integrated instrument system, the above warranty shall not be applicable, and this product shall be covered only by the system warranty.

Service contracts or customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

SECTION IX H

75 MHz TIMER/COUNTER

5308A

OPERATING AND SERVICE MANUAL

SERIAL PREFIX: 1528A

This section applies directly to Model 5308A 75 MHz Timer/Counters having Serial Prefix 1528A. The section is provided in loose-leaf form for incorporation into the 5300B Measuring System Manual.

NEWER INSTRUMENTS

This section with enclosed "Manual Changes" sheet applies directly to HP Model 5308A 75 MHz Timer/Counters having Serial Prefix numbers above 1528A.

OLDER INSTRUMENTS

Subsection VII of this document contains information pertinent to all older instruments with Serial Prefix 1440A or 1524A.

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SECTION IX H
5308A 75 MHz TIMER/COUNTER

SUBSECTION I
GENERAL INFORMATION

9H-1-1. PURPOSE AND USE OF SECTION IX H

9H-1-2. Section IX H contains the information necessary to install, operate, and maintain the HP 5308A Timer/Counter. Theory of operation, parts lists, component locator illustrations, and a schematic diagram are included. Insert this document in the HP 5300B Measuring System manual as part of Section IX.

9H-1-3. INSTRUMENT DESCRIPTION

9H-1-4. When plugged onto a 5300B mainframe, the 5308A can measure frequency, frequency ratio, period, period average, time interval, and time interval average. A single-channel or a two-channel totalize function is provided. The two-channel function totalizes pulses on Channel A during pulses on Channel B or between pulses on Channel B.

9H-1-5. Front panel controls are provided for function and time base selection and for signal conditioning (slope, level, and attenuation). Automatic selection of maximum resolution is provided for the four functions of frequency, frequency ratio, period average, and time interval average measurements. Trigger indicator lamps are provided to indicate when internal amplifier triggering occurs.

9H-1-6. Rear panel connectors provide a gate output for Z axis modulation of an oscilloscope, trigger level outputs for monitoring the voltage level at which each channel triggers, and a time base output for use in totalizing, period, and time interval measurements.

9H-1-7. The electrical and mechanical specifications are listed in Table 9H-1-1.

9H-1-8. INSTRUMENT IDENTIFICATION

9H-1-9. Hewlett-Packard uses a two-section, nine-digit serial number (0000A00000) mounted on the rear panel to identify the instrument. The first four digits are the serial prefix and the last five digits refer to the specific instrument. If the serial prefix on your instrument differs from that listed on the title page of this section, there are differences between the manual and your instrument. Lower serial prefixes are covered by a manual change sheet included with the manual.

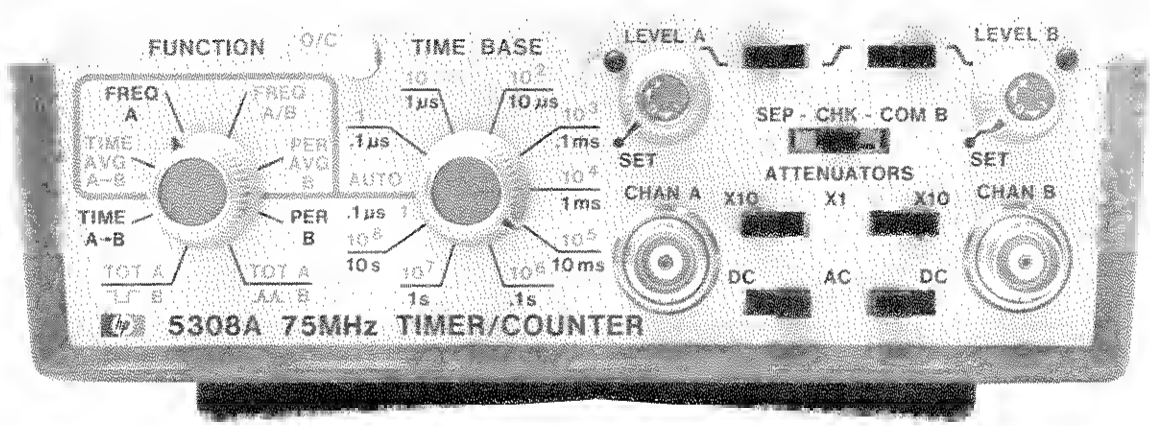


Figure 9H-1-1. 5308A 75 MHz Timer/Counter

9H-1-10. The printed circuit board within the instrument is identified by a two-section, 10-digit part number (e.g., 05308-60001) and a four-digit series number (e.g., "SERIES 1440A"). The series number identifies the electrical characteristics of the complete printed-circuit assembly. A replacement circuit-board assembly may have a different series number than the assembly originally supplied with the instrument. Therefore, when troubleshooting a circuit-board assembly, ensure that the series number on the schematic diagram matches the series number on the board assembly. If the series number on the assembly is lower than the number on the schematic diagram in Subsection VIII, refer to Subsection VII of this document for change information. If the series number on the assembly is higher than the number on the schematic diagram in Subsection VIII, tbe change information is provided in a manual change sheet which is available from the nearest Hewlett-Packard Sales and Service Office.

9H-1-11. Manual Changes and Options

9H-1-12. The title page lists the serial prefix number to which this manual directly applies. If the serial prefix is different from the one listed, a change sheet is included describing the required changes. If this change sheet is missing, the information can be supplied by any Hewlett-Packard Sales and Service office listed in Section VIII of the 5300B Measuring System manual. Options are listed in Section IX H, Subsection VII.

Table 9H-1-1. Specifications

INPUT CHANNELS A AND B

RANGE: DC Coupled; 0 to 75 MHz
AC Coupled; 20 Hz to 75 MHz

SENSITIVITY: (Min) 25 mV rms sine wave to 10 MHz. 50 mV rms sine wave to 75 MHz. 150 mV p-p pulse at minimum pulse width of 10 ns. Input must be less than 1V rms from 50 to 75 MHz with Attenuator switch in X1 position. Sensitivity can be decreased by 10 using Attenuator switch.

IMPEDANCE: 1 MΩ shunted by less than 48 pF.

OVERLOAD PROTECTION: †

DC Range:

X1:	DC to 400 kHz	125V rms
	400 kHz to 5 MHz	Vrms = $(5x10^7) \div (Hz)$
	5 MHz to 75 MHz	10V rms
X10:	DC to 4 MHz	250V rms
	4 MHz to 75 MHz	Vrms = $(1x10^9) \div (Hz)$

AC Ranges:

DC to 10 Hz	200V peak in addition to above ratings.

TRIGGER LEVEL: Set position centers triggering at 0 volts, or continuously variable over the range of ±2.0V with Attenuator in X1 position or ±20V with Attenuator in X10 position. Trigger level available on rear panel BNC connectors for DVM monitoring.

SLOPE: Independent selection of triggering on positive or negative slope.

CHANNEL INPUTS: Separate or Common B

GATE OUTPUT: Rear panel BNC. TTL low level while gate is open may be used to intensity modulate an HP oscilloscope.

TIME BASE/SCALING OUTPUT: Available at rear panel BNC.

FREQUENCY

RANGE: 0 to 75 MHz, Channel A or Channel B.

GATE TIMES: 8 manually selectable times from 1 μs to 10 seconds. AUTO position selects gate time for maximum resolution within a 1.1 second measurement time.

ACCURACY: ±1 count ± time base accuracy.

DISPLAY: Hz, kHz, and MHz with positioned decimal point.

FREQUENCY RATIO

DISPLAY: Fa/Fb, measured over N periods of Fb. N=1 to 10^8, selectable in decade steps with automatic decimal position and annunciators. AUTO position selects N automatically for maximum resolution within a 1.1 second measurement time.

RANGE: Channel A; 0 to 75 MHz. Channel B; 0 to 5 MHz.

ACCURACY: ±1 count of Fa ± trigger error of Fb*.

PERIOD

RANGE: 0 Hz to 5 MHz, Channel B

RESOLUTION: 100 ns to 10 s in decade steps.

ACCURACY: ±1 count ± time base accuracy ± trigger error*.

DISPLAY: μs, or s with positioned decimal point.

PERIOD AVERAGE

RANGE: 0 to 5 MHz; (100 ns to 10 s), Channel B.

PERIODS AVERAGED: 1 to 10^8 manually selectable in decade steps. AUTO position automatically selects number of periods for maximum resolution within a 1.1 second measurement time.

FREQUENCY COUNTED: 10 MHz.

ACCURACY: ±1 count ± time base accuracy ± trigger error*.

DISPLAY: mμs (ns), μs, with positioned decimal points. (In the 10^8 position of the TIME BASE switch, the display will be ps with no annunciator shown.)

TIME INTERVAL

RANGE: 200 ns to 10^9 s. 25 ms minimum pulse width. Separate or Common B.

RESOLUTION: 100 ns to 10 s in decade steps.

ACCURACY: ±1 count ± time base accuracy ± trigger error*.

DISPLAY: μs, s, or ks with positioned decimal point.

TIME INTERVAL AVERAGE

RANGE: 1 ns to 10 s. 200 ns dead time between intervals. Channels A and B separate or Common B.

INTERVALS AVERAGED: 1 to 10^8 selectable in decade steps. AUTO position selects number of intervals to give maximum resolution within a measurement time of 1.1 second.

DISPLAY: mμs (ns), μs, or s with positioned decimal point. (In the 10^8 position of the TIME BASE switch, the display will be in ps with no annunciator shown.)

ACCURACY: ± time base accuracy ±5 ns

$$\frac{\pm\,[\text{Trigger Error}^* \pm 100\text{ ns}]}{\sqrt{\text{Intervals Averaged}}}$$

TOTALIZE

Totalizes Channel A during pulses on Channel B.
Totalizes Channel A between pulses on Channel B.

RANGE: 75 MHz on Channel A in position 1 of TIME BASE switch, 5 MHz in other positions of TIME BASE switch.

ACCURACY: ±1 count ± trigger error on Channel B*.

DISPLAY: Displays count. Can scale display with annunciator by use of TIME BASE switch to increase count capacity.

GENERAL

NOTE: 5308A is compatible with 8 digit 5300B mainframe only.

CHECK: Inserts internal 10 MHz reference frequency into counting decades. Displays 10^N counts for TIME BASE switch positions 10 through 10^8 with proper decimal position and annunciator.

OPERATING TEMPERATURE: 0° to 50°C.

POWER REQUIREMENTS: Including 5300B mainframe, nominally 15 watts.

WEIGHT: Net, 0.9 kg (2 lb). Shipping, 1.5 kg (3¼ lb).

DIMENSIONS: With mainframe 89 mm H (3½") x 760 mm W (6¼") x 248 mm L (9¾").

†SEE WARNING ON PAGE 9H-3-11.

*For any waveshape, trigger error (μs) is less than ±

$$\frac{0.005}{\text{Signal Slope (V/}\mu\text{s)}}$$

For period average, this is less than ±0.3% of one period ÷ periods averaged for signals with 40 dB or better signal-to-noise ratio.

SECTION IX H
5308A 75 MHz TIMER/COUNTER

SUBSECTION II
INSTALLATION

9H-2-1. INTRODUCTION

9H-2-2. This section contains information on unpacking and inspection, storage and shipment, installation and removal of plug-on, and portable operation.

9H-2-3. UNPACKING AND INSPECTION

9H-2-4. If the shipping carton is damaged, ask that the carrier's agent be present when the instrument is unpacked. Inpsect the instrument for damage such as scratches, dents, broken knobs, etc. If the instrument is damaged or fails to meet performance tests when used with the 5300B mainframe, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. Performance check procedures are located in Subsection V, and Sales and Service Offices are listed in Section VI of the 5300B portion of the manual. Retain tbe shipping carton and the padding material for the carrier's inspection. The Sales and Service Office will arrange for the repair or replacement of the instrument without waiting for the claim against the carrier to be settled.

9H-2-5. STORAGE AND SHIPMENT

9H-2-6. PACKAGING. To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Your Hewlett-Packard Sales and Service Office can provide packaging material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable custom packaging on short notice. The unit was originally packaged as follows:

> The original container is a corrugated cardboard box with 200 lbs. burst test (HP 9211-1620). The instrument is secured and protected in the box by a top and bottom molded frame of polystyrene foam (HP No. 9220-1545).

9H-2-7. ENVIRONMENT. Conditions during storage and shipment should normally be limited as follows:

a. Maximum altitude: 25,000 feet.
b. Minimum temperature: -40°F (-40°C).
c. Maximum temperature: +167°F (+75°C).

9H-2-8. INSTALLATION AND REMOVAL OF PLUG-ON

9H-2-9. The counter must be used with a 5300B mainframe to make measurements. Mate the counter and the mainframe according to the instructions given in Paragraph 2-11 and Figure 2-1 in the 5300B mainframe documentation.

9H-2-10. PORTABLE OPERATION

9H-2-11. Use of the HP Model 5310A Battery Pack enables the 5300B mainframe and the counter to be used in areas removed from ac power sources. The battery pack provides a minimum of 3 hours operation (typically 5 hours) at 20° to 30°C operating and charging temperature. Tables 1-2 and 1-4 of the 5300B portion of the manual lists tbe battery pack as an available accessory. Documentation for the battery pack is also included in Section IV through VIII of the 5300B portion of the manual. To prepare the 5300B/5308A for portable operation, refer to Paragraph 2-13 and Figure 2-2, of the 5300B portion of the manual.

SECTION IX H
5308A 75 MHz TIMER/COUNTER

SUBSECTION III
OPERATION

9H-3-1. INTRODUCTION

9H-3-2. This section provides operating information and describes modes of operation and operating procedures. The 5308A plug-on may he used to measure frequency or frequency ratio up to 75 MHz, period to 5 MHz, period average to 5 MHz, time interval from 200 nanoseconds to 10 seconds and time interval average from 1 nanosecond to 10^9 seconds. Signals up to 75 MHz may be totalized on Channel A in the single-channel totalize function. In the two-channel totalize function, signals up to 75 MHz may be totalized on Channel A during pulses on Channel B or between pulses on Channel B.

9H-3-3. OPERATING INFORMATION

9H-3-4. The front panel contains a FUNCTION selector, a TIME BASE selector and signal conditioning controls for use with the Channel A and Channel B input connectors. The signal conditioning controls are labeled LEVEL A and LEVEL B, ATTENUATORS and AC-DC. An O/C (open/close) switch is provided for Channel B and a SEP-CHK-COM B switch is provided for selecting channel inputs and self check function. The purpose and use of these controls is described in the following paragraphs.

9H-3-5. Function Selector

9H-3-6. The FUNCTION selector selects one of the eight operating modes listed in paragraph 9H-3-2.

9H-3-7. Time Base Selector

9H-3-8. The TIME BASE selector provides gate time control for frequency measurements, resolution settings for period or time interval mode, selection of number of cycles averaged during frequency ratio, period average, or time interval average modes, and provides a scaling factor of 1 to 10^8 in the totalize mode. The AUTO position automatically sets the TIME BASE selection (for maximum resolution within 1.1 second measurement time) for frequency gate time, and for number of cycles averaged in ratio, period average and time interval average measurements.

9H-3-9. Signal Conditioning Controls

9H-3-10. Four types of signal conditioning controls are provided for each channel (A and B) input. These controls allow adjustment of trigger level and selection of attenuation, slope and ac or dc coupling. The effect of these controls is to minimize inaccuracies in measurements (refer to Figure 9H-3-1).

9H-3-11. ATTENUATORS. X1 and X10 positions (both channels). The X10 position of the attenuator switch is used to attenuate large amplitude signals. The X1 position represents no attenuation. The switch setting X10 increases the trigger levels and hysteresis voltages by a factor of 10. If input signal levels are unknown, the initial measurements should be made with the attenuator switches set to X10. The setting may then be changed to X1 if necessary to obtain a stable, usable measurement.

9H-3-12. SLOPE SWITCHES (both channels). The slope switches allow triggering on the positive slope or the negative slope of the input signals (see Figure 9H-3-1).

9H-3-13. LEVEL A and LEVEL B. The level controls allow adjustment of the triggering point on the input signal waveform. With the LEVEL controls set to tbe "0" position (or to the SET position when the rear panel 'SET' TRIG LEVELS switch is in the .0V position as described in Figure 9H-3-3) triggering is centered around zero volts. The voltage range over which triggering may be set is ±2 volts with the attenuators in the X1 position or ±20 volts with the attenuator switch in the X10 position.

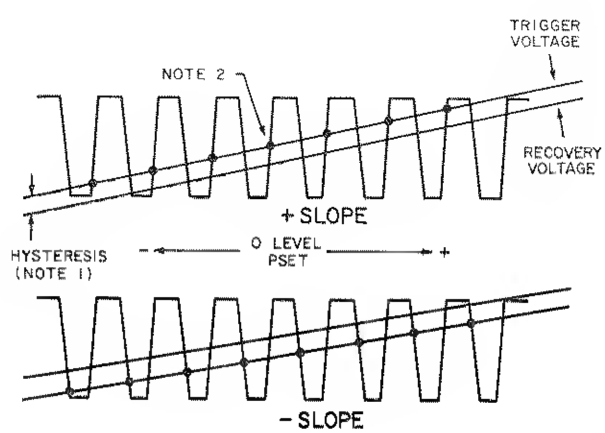
9H-3-14. AC-DC SWITCHES (both channels). The AC-DC switches select ac or dc coupling. In AC position with the LEVEL control set for triggering centered around zero ac volts, the dc components on the signal have no effect. In DC position with the LEVEL control in SET (as described in the preceding paragraph) triggering is centered around zero volts dc.

9H-3-15. O/C (open/close) Switch

9H-3-16. This pushbutton switch controls totalizing of Channel A input signals as described in paragraph 9H-3-34. This switch also controls the stopwatch function as described in paragraph 9H-3-40.

9H-3-17. SEP-CHK-COM B Switch

9H-3-18. This switch provides selection of separate Channel A and Channel B inputs in the SEP position. The CHK position enables the self check function as described in paragraph 9H-3-39 and the stopwatch function as described in paragraph 9H-3-41. The COM B position connects the CHAN B connector on the front panel to the Channel A and Channel B amplifier circuits in parallel.



1. HYSTERESIS (NOISE REJECTION) VOLTAGE IS CONSTANT FOR EACH ATTENUATOR SETTING AND DOES NOT VARY WITH TRIGGER LEVEL
2. THIS ALLOWS ZERO VOLTS TRIGGERING WITH GOOD NOISE REJECTION
3. ATTENUATOR: X1, X10 CHANGES TRIGGER LEVEL AND HYSTERESIS VOLTAGES BY FACTOR OF 1, 10.

Figure 9H-3-1. Signal Conditioning Using Attenuator, Level and Slope Controls

9H-3-19. MODES OF OPERATION

9H-3-20. The 5308A provides seven modes of operation in addition to a self-check function and a stopwatch function. Some modes of operation are available on both channels (A or B) while other modes are available on only one channel. In all cases, the modes are selected by the FUNCTION switch. The modes and functions are:

a. Frequency Mode (Channel A or B).

b. Frequency Ratio Mode (Channel A/B).

c. Period Mode (Channel B only).

d. Period Average Mode (Channel B only).

e. Time Interval Mode (Channel A to B or Channel B only).

f. Time Interval Average Mode (Channel A to B or Channel B only).

g. Totalize Mode (Single or two channel).

h. Self Check Function.

i. Stopwatch Function.

9H-3-21. Frequency Mode (Channel A or B)

9H-3-22. Frequency measurements may be made on Channel A or B from 0 to 75 MHz. Front panel controls are set to the same relative positions for measurements on either channel with the exception that the SEP-CHK-COM B switch is set to SEP for Channel A and to COM B for Channel B measurements. The LEVEL A control adjusts the triggering point on the input signal for Channel A or Channel B in the frequency mode. Accuracy is ±1 count ± time base accuracy.

9H-3-23. Frequency Ratio Mode (Channel A/B)

9H-3-24. The frequency ratio of Channel A signals (from 0 to 75 MHz) to Channel B signals (0 to 5 MHz) can be measured. The TIME BASE switch setting (1 to 10^8) selects the number of cycles of the Channel B signal over which the ratio A/B is averaged. Accuracy is ±1 count of Frequency A ± trigger error of Frequency B. Increasing the number of cycles of Frequency B (higher setting of TIME BASE switch) results in increased accuracy.

9H-3-25. Period Mode (Channel B)

9H-3-26. The period mode allows single period measurements to be made with frequencies of 0 to 5 MHz into Channel B. The resolution is selectable from 100 nanoseconds to 10 seconds by the TIME BASE switch. Accuracy is ±1 count ± time base accuracy ± trigger error.

9H-3-27. Period Average Mode (Channel B)

9H-3-28. The period average mode allows multiple period averages to be made with frequencies of 0 to 5 MHz into Channel B. The number of periods to be averaged is selected by the TIME BASE switch (1 to 10^8). Accuracy is ±1 count ± time base accuracy ± trigger error. The ± 1 count and trigger error is reduced in proportion to the number of periods averaged.

9H-3-29. Time Interval Mode (Channel A to B or Channel B only)

9H-3-30. The time interval mode allows time measurements to be made between points on one waveform or between two waveforms. The range of measurements is 200 nanoseconds to 10^9 seconds (minimum pulse width of 25 nanoseconds) with resolution of 100 nanoseconds to 10 seconds in decade steps. A Start signal (Channel A) opens the main gate and a Stop signal (Channel B) closes it. (For Start and Stop signals from a common source, the CHAN B input is used and the SEP-CHK-COM B switch is set to COM B.) A TTL low output is available at the GATE OUT connector on the rear panel while the gate is open. This output is

used to intensity modulate an oscilloscope for display of the time interval measured. Accuracy is ± 1 count ± time base accuracy ± trigger error. For more precise measurement of trigger level, connectors are provided on the rear panel for DVM monitoring of the trigger level voltage.

9H-3-31. Time Interval Average Mode (Channel A to B or Channel B Only)

9H-3-32. The time interval average mode provides greater resolution of time interval measurements than the time interval mode provides. The ± 1 count error can be reduced by averaging a number of measurements. In the time interval average mode, the main gate is open for the number of time intervals selected by the TIME BASE switch. Up to 10^8 time intervals may be averaged in this mode. Since the measurement accuracy is increased by $\frac{1}{\sqrt{N}}$ (instead of $\frac{1}{N}$ as shown on the display) the displayed measurement should be evaluated by computing the true resolution which is $\frac{\pm 100\ \text{ns}}{\sqrt{N}}$ where N is equal to the number of time intervals selected by the TIME BASE switch. For detailed information on time interval averaging, refer to HP Application Note 162-1.

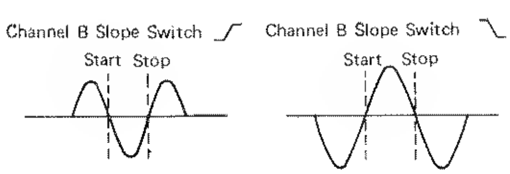
9H-3-33. Totalize Mode (Single or Two Channel)

H-3-34. Input signals up to 75 MHz applied to Channel A can be totalized with the TIME BASE switch in position 1. In all other positions of the TIME BASE switch input signals up to 5 MHz can be totalized. The input frequency is scaled by a factor equal to the setting of the TIME BASE switch (10^N).

9H-3-35. For single-channel totalizing, the Channel A signal is totalized under control of the O/C switch when the FUNCTION switch is in the TOT A, ⊓⊓ B position. Totalizing is initiated by pressing the O/C switch and terminated by pressing the O/C switch a second time.

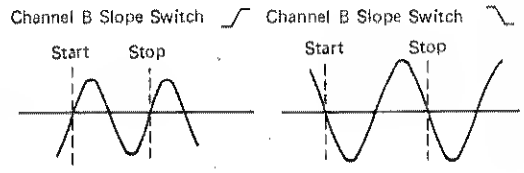
9H-3-36. For two-channel totalizing, the Channel A signal is totalized under control of the Channel B signal. When the FUNCTION switch is in the TOT A, ⊔ B position (totalize Channel A during pulses on Channel B) the Start and Stop signals on Channel B occur between two successive trigger level crossings in the opposite direction, as follows:

FUNCTION
TOT A, ⊔ B



9H-3-37. When the FUNCTION switch is in the TOT A, ⊓⊓ B position (totalize Channel A between pulses on Channel B) the Start and Stop signals on Channel B occur between two successive trigger level crossings in the same direction as follows:

FUNCTION
TOT A, ⊓⊓ B



9H-3-38. Self Check Function

9H-3-39. The CHK position of the SEP-CHK-COM B switch on the front panel provides a position where proper operation of the majority of the logic circuits in the 5308A and 5300B is verified. When circuits are functioning properly, the 10^N counts are displayed for positions 10 through 10^8 of the TIME BASE switch with the proper decimal position and annunciator.

9H-3-40. Stopwatch Function

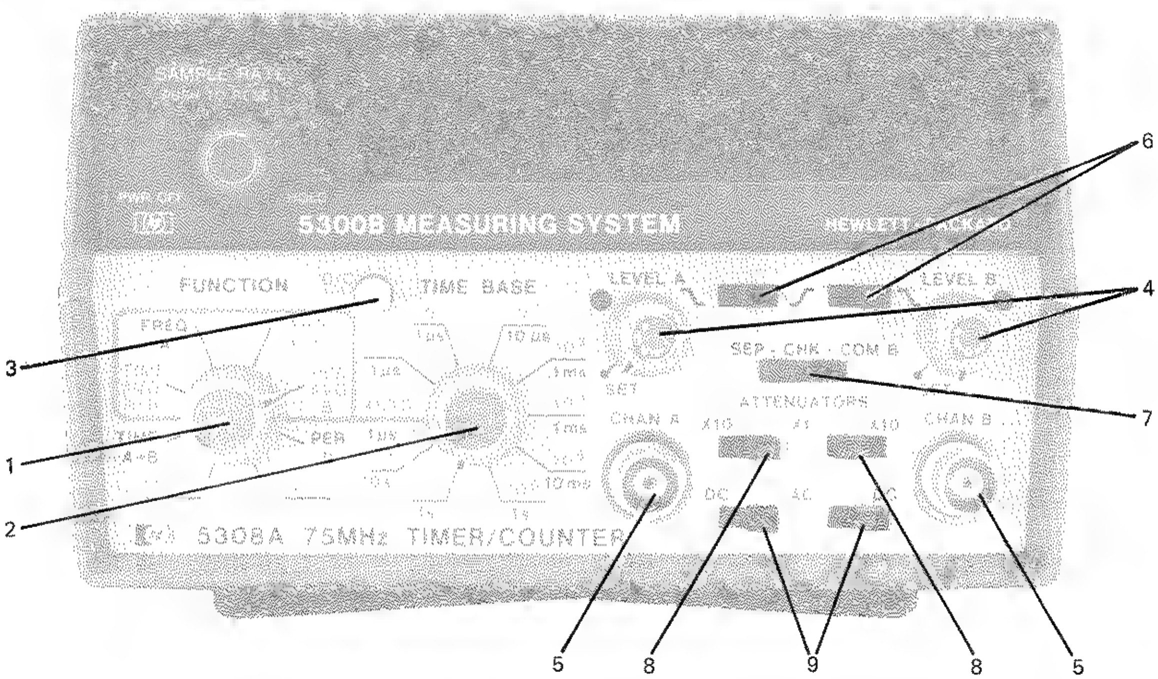
9H-3-41. The CHK position of the SEP-CHK-COM B switch also provides an electronic stopwatch function when the FUNCTION switch is set to TOT A, ⊓⊓ B. After the RESET switch is pressed, the stopwatch count is started by pressing the O/C switch. The count is terminated by pressing the O/C switch a second time. To initiate a new measurement, the RESET switch must be pressed.

9H-3-42. CONTROLS AND CONNECTORS

9H-3-43. The front panel controls and connectors are described in Figure 9H-3-2 and the rear panel switch and connectors are described in Figure 9H-3-3.

9H-3-44. OPERATING PROCEDURES

9H-3-45. The operating procedures for making measurements in the various modes are listed in Figures 9H-3-4 through 9H-3-12.



1. FUNCTION. Eight position switch selects mode of operation, as follows (blue lettering matches corresponding blue lettering on TIME BASE switch):

   a. FREQ A. Enables frequency measurements of 0 to 75 MHz to be made using Channel A.

   b. FREQ A/B. Enables the frequency ratio of Channel A signals to Channel B signals to be taken. The ratio of Channel A input signals (from 0 to 75 MHz) to the Channel B input signals (0 to 5 MHz) can be measured. The ratio is averaged over N cycles of the Channel B signal. N is selectable from 1 to 10^8 by the TIME BASE switch. Accuracy is ±1 count of frequency A, ± trigger error of Frequency B.

   c. TIME AVG A→B. Sets counter to measure average time interval, A to B. Channel A starts the interval and Channel B stops the interval. The TIME BASE switch (blue lettering) sets the number of time intervals to be averaged. Time interval input range is 1 ns to 10 s; there must be a 200 ns deadtime between intervals.

   d. TIME A→B. Sets counter to measure time interval A to B. Channel A starts the measurement and Channel B stops the measurement. Time interval input range is 200 ns to 10^9 s (25 ns minimum pulse width). The TIME BASE switch (black lettering) selects resolution of 100 ns to 10 s.

   e. PER AVG B. Enables multiple period averages to be made from Channel B with frequencies of 0 to 5 MHz (range of 200 ns to 10 s). Use TIME BASE switch (blue lettering) to select number of periods to be averaged (1 to 10^8).

   f. PER B. Enables single period measurements to be made from Channel B with frequencies of 0 to 5 MHz. The TIME BASE switch (black lettering) selects resolution of 100 ns to 10 s.

   g. TOT A, ⊔ B. Totalizes signals on Channel A during pulses on Channel B. (Refer to paragraph 9H-3-33.) Totalizes signals up to 75 MHz with TIME BASE switch in position 1 (blue lettering), up to 5 MHz with TIME BASE switch in any other position (10^N).

Figure 9H-3-2. Front Panel Controls and Connectors

h. TOT A, ⊓⊓ B. Totalizes Channel A between pulses on Channel B. (Refer to paragraph 9H-3-33.) Totalizes signals up to 75 MHz with TIME BASE switch in position 1 (blue lettering), up to 5 MHz with TIME BASE switch in any other position (10^N).

2. TIME BASE. Ten position switch performs the following functions:

a. 1 μs, 10 μs, .1 ms, 1 ms, 10 ms, .1 s, 1 s, 10 s (black lettering). Provides eight selectable times as gate time controls for frequency (FREQ A) measurements.

b. .1 μs, 1 μs, 10 μs, .1 ms, 1 ms, 10 ms, .1 s, 1 s, 10 s (black lettering). Provides resolution of 100 ns to 10 s when FUNCTION switch selects period (PER B) or time interval (TIME A→B) mode of operation.

c. 1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7, 10^8, (blue lettering). Provides selection of number of cycles or events averaged when FUNCTION switch selects frequency ratio (FREQ A/B), period average (PER AVG B), or time interval average (TIME AVG A→B).

d. 1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7, 10^8, (blue lettering). Provides scaling factor when FUNCTION switch selects totalize (TOT A, ⊔ B/TOT A, ⊓⊓ B) modes of operation.

e. AUTO/.1 μs 1. The AUTO position provides four function auto-ranging (pertains to gray-bordered FUNCTION switch positions) including frequency (FREQ A), frequency ratio (FREQ A/B), period average (PER AVG B) and time interval average (TIME AVG A→B). Provides maximum resolution that can be obtained in each function within a maximum of 1.1 second measurement time.

f. AUTO/.1 μs 1. The .1 μs 1 position pertains to the FUNCTION switch lower-half positions (corresponding letter colors). The .1 μs position (black lettering) pertains to TIME A→B and to PER B. The 1 position (blue lettering) pertains to TOT A, ⊔ B and to TOT A, ⊓⊓ B.

3. O/C (open/close). Pushbutton switch enables input signals to Channel A to be totalized when the FUNCTION switch selects TOT A, ⊓⊓ B. Totalizing is initiated by pressing tbe O/C switch and is terminated by pressing the switch a second time. To reinitiate the totalize function the reset switch on the front panel of the 5300B mainframe must be pressed. An additional function of the O/C switch is to operate the display as a stop-watch (see Figure 9H-3-12).

4. LEVEL A and LEVEL B. Used in conjunction with ATTENUATORS switch to determine voltage at which triggering occurs for Channel A or Channel B. In SET position, triggering is centered around 0 volts when the rear panel 'SET' TRIG LEVELS switch is in the .0V position. Trigger level is continuously variable over the range of ±2V (ATTENUATORS IN X1) or ±20V (ATTENUATORS in X10). Adjacent lamp indicates when amplifier triggering occurs.

5. CHAN A and CHAN B. Input connectors for Channel A and Channel B. Input impedance is 1MΩ shunted by less than 48 pF. By using a 10 to 1 divider probe, input impedance can be increased to 10 MΩ.

6. Slope Switch. Selects the triggering on positive or negative slope of the input signals to Channel A (switch on left side) or Channel B (switch on right side).

7. SEP-CHK-COM B. (Separate-Check-Common B).

a. SEP. Channel A and Channel B are connected for separate source inputs (1 MΩ input impedance).

b. CHK. Self check verifies that the majority of the 5300B mainframe logic circuits and the 5308A logic circuits are functioning properly.

c. COM B. Disconnects front panel input connector CHAN A and connects CHAN B to the amplifiers for Channel A and Channel B in parallel (1MΩ input impedance).

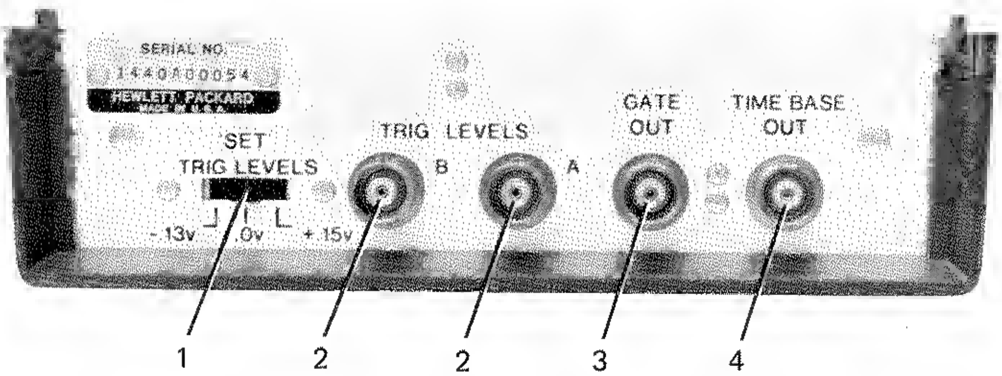
8. ATTENUATORS. Selects attenuation of the input signals to Channel A (switch on left side) and to Channel B (switch on right side).

a. X1 connects input signals directly to input amplifiers.

b. X10 attenuates input signals by a factor of 10.

9. AC-DC. Selects ac coupling or dc coupling of the input signals to Channel A (switch on left side) or Channel B (switch on right side).

Figure 9H-3-2. Front Panel Controls and Connectors (Cont'd)



1. 'SET' TRIG LEVELS. Three position switch presets the trigger level to the indicated voltage (-.13V, .0V, +.15V) when the LEVEL control on the front panel is in the SET position. With a 10:1 divider probe connected to the CHAN A or CHAN B connector on the front panel, the -.13V position is used when checking ECL logic circuits and the +.15V position is used when checking TTL logic circuits. The .0V position is used when measuring a symmetrical waveform such as a sine wave.

2. TRIG LEVELS A and B. Connectors provide for measurement of Channel A or Channel B trigger levels by a monitoring DVM. The trigger level voltage is measured at the midpoint of the hysteresis band.

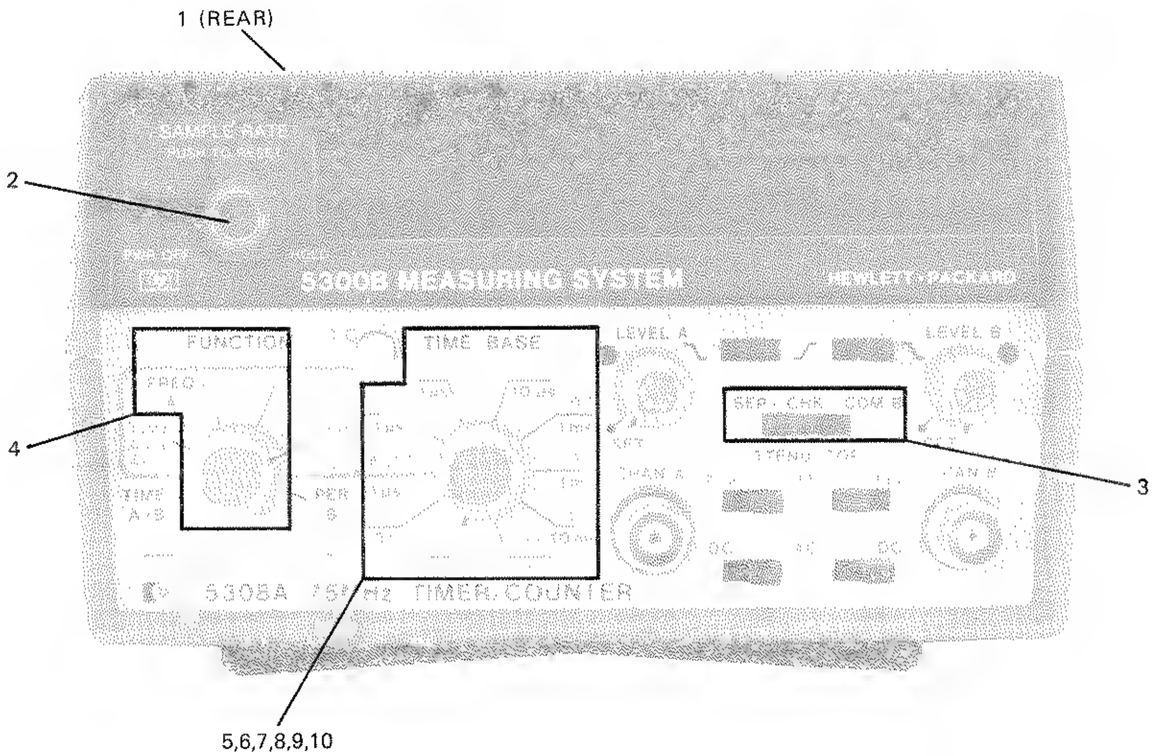
3. GATE OUT. Provides a TTL level signal (LOW) while the 5300B main gate is open. Used for time interval measurements to intensity modulate an oscilloscope to indicate the interval being measured.

4. TIME BASE OUT. This connector provides two different outputs, selectable by the position of the FUNCTION switch, as follows:

   a. In the TOT A, ⊓⊔⊓ B and TOT A, ⋀⋀ B positions of the FUNCTION switch, the TIME BASE OUT connector provides a scaled (divided) output of the input signal frequency applied to Channel A. The output is scaled by a factor of from 10 to 10^8 as set on the TIME BASE control.

   b. In the PER B and TIME A→B positions of the FUNCTION switch, the TIME BASE OUT connector provides a scaled output of the internal 10 MHz oscillator frequency. The output is scaled by a factor of from 10 to 10^8 as set on the TIME BASE control. The period of this output is indicated by the black lettering on the TIME BASE control. The same output is provided when the FUNCTION switch is in TOT A, ⊓⊔⊓ B or TOT A, ⋀⋀ B position and the SEP-CHK-COM B switch is in the CHK position.

Figure 9H-3-3. Rear Panel Control and Connectors



NOTE

If proper indications are not received during the self check, refer to the trouble-shooting procedures in Section V.

1. Connect ac power to 5300B ac receptacle.
2. Turn ac power on with 5300B SAMPLE RATE control. Adjust SAMPLE RATE for desired display time.
3. Set the SEP-CHK-COM B switch to CHK

NOTE

All display indications are ±1 count. In the 10^8 position of the TIME BASE switch, wait 10 seconds for the count display.

4. Set the FUNCTION switch to FREQ A.
5. Set the TIME BASE switch to the positions listed below and observe the display.

Frequency A Self Check

TIME BASE	DISPLAY	ANNUNCIATOR
AUTO	10000.000	kHz
.1 μs	10000.000	kHz
1 μs	00000010	MHz
10 μs	0000010.0	MHz
.1 ms	000010.00	MHz
1 ms	00010.000	MHz
10 ms	0010000.0	kHz
.1 s	010000.00	kHz
1 s	10000.000	kHz
10 s	•0000000.0	Hz

• = OVERFLOW

Figure 9H-3-4. Making Self Check Measurements

Ratio Self Check

6. Set the FUNCTION switch to FREQ A/B. Set the TIME BASE switch as shown below and observe the display.

TIME BASE	DISPLAY	ANNUNCIATOR
AUTO	1000000.0	μ
1	10000000	
10	0000001.0	
10^2	000001.00	
10^3	00001.000	
10^4	0001.0000	
10^5	001.00000	
10^6	01000000	μ
10^7	1000000.0	μ
10^8	•000000.00	μ

• = Overflow

Period Average Self Check

7. Set the FUNCTION switch to PER AVG B. Set the TIME BASE switch as shown below and observe the display.

TIME BASE	DISPLAY	ANNUNCIATOR
AUTO	100.00000	Mμs
1	1000000.0	μs
10	000000.10	μs
10^2	00000.100	μs
10^3	0000.1000	μs
10^4	000.10000	μs
10^5	00100.000	Mμs
10^6	0100.0000	Mμs
10^7	100.00000	Mμs
10^8	•00000.000	

• = Overflow

Mμs = Nanoseconds

Period Self Check

8. Set the FUNCTION switch to PER B. Set the TIME BASE switch as shown below and observe the display.

TIME BASE	DISPLAY	ANNUNCIATOR
AUTO	1000000.0	μs
.1 μs	1000000.0	μs
1 μs	00000010	μs
10 μs	000.00100	s
.1 ms	0000.1000	s
1 ms	00010.000	s
10 ms	001000.00	s
.1 s	0100000.0	s
1 s	10000000	s
10 s	•000000.00	ks

• = Overflow

Time Interval Self Check

9. Set the FUNCTION switch to TIME A→B. Set the TIME BASE switch as shown below and observe the display.

TIME BASE	DISPLAY	ANNUNCIATOR
AUTO	1000000.5	μs
.1 μs	1000000.5	μs
1 μs	00000015	μs
10 μs	000.00105	s
.1 ms	0000.1005	s
1 ms	00010.005	s
10 ms	001000.05	s
.1 s	0100000.5	s
1 s	10000005	s
10 s	•000000.05	Ks

• = Overflow

Time Interval Average Self Check

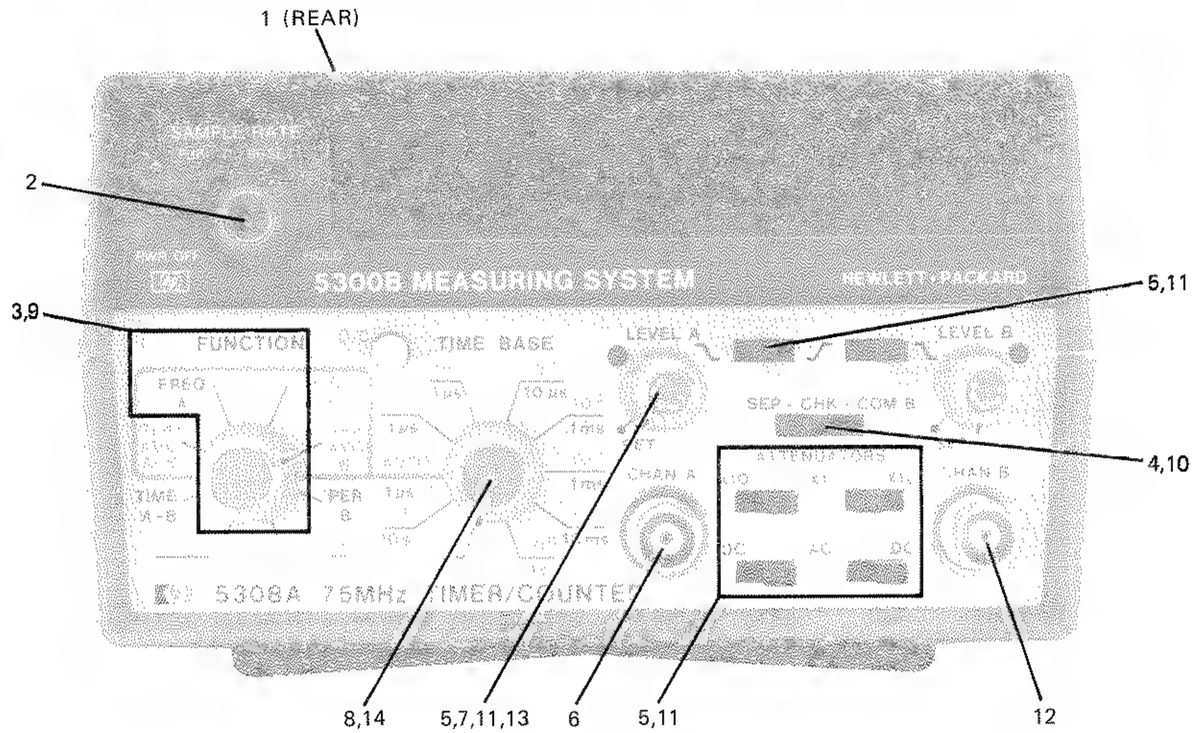
10. Set the FUNCTION switch to TIME AVG A→B. Set the TIME BASE switch as shown below and observe the display.

TIME BASE	DISPLAY	ANNUNCIATOR
AUTO	100.00000	Mμs
1	1000000.0	μs
10	000000.10	μs
10^2	00000.100	μs
10^3	0000.1000	μs
10^4	000.10000	μs
10^5	00100.000	Mμs
10^6	0100.0000	Mμs
10^7	100.00000	Mμs
10^8	•00000.000	

• = Overflow

Mμs = Nanoseconds

Figure 9H-3-4. Making Self Check Measurements (Cont'd)



SEE WARNING ON PAGE 9H-3-11

1. Connect ac power to 5300B ac receptacle.
2. Turn ac power on with the 5300B SAMPLE RATE control.

Channel A

3. Set FUNCTION to FREQ A and adjust SAMPLE RATE for desired display time.
4. Set SEP-CHK-COM B to SEP.
5. Set ATTENUATORS to X10; AC-DC to AC and Channel A slope switch to polarity desired. Set LEVEL A to SET.

NOTE

Ensure that the 'SET' TRIG LEVELS switch on the rear panel is in the .0V position when the LEVEL control is in the SET position.

6. Connect input signal (up to 75 MHz) to be measured to CHAN A connector.
7. Observe display. If display is not stable, rotate LEVEL A control until trigger light illuminates. If necessary, set ATTENUATORS switch for Channel A to X1.
8. Set TIME BASE to desired gate time or to AUTO.

Channel B

9. Set FUNCTION to FREQ A and adjust SAMPLE RATE for desired time.
10. Set SEP-CHK-COM B to COM B.

NOTE

In the Frequency mode of operation, the CHAN B input is processed by the Channel A amplifier circuit. Consequently, the slope and LEVEL controls for Channel A are effective as listed below. The Channel B ATTENUATORS and AC-DC switches are effective (see Figure 9H-8-1).

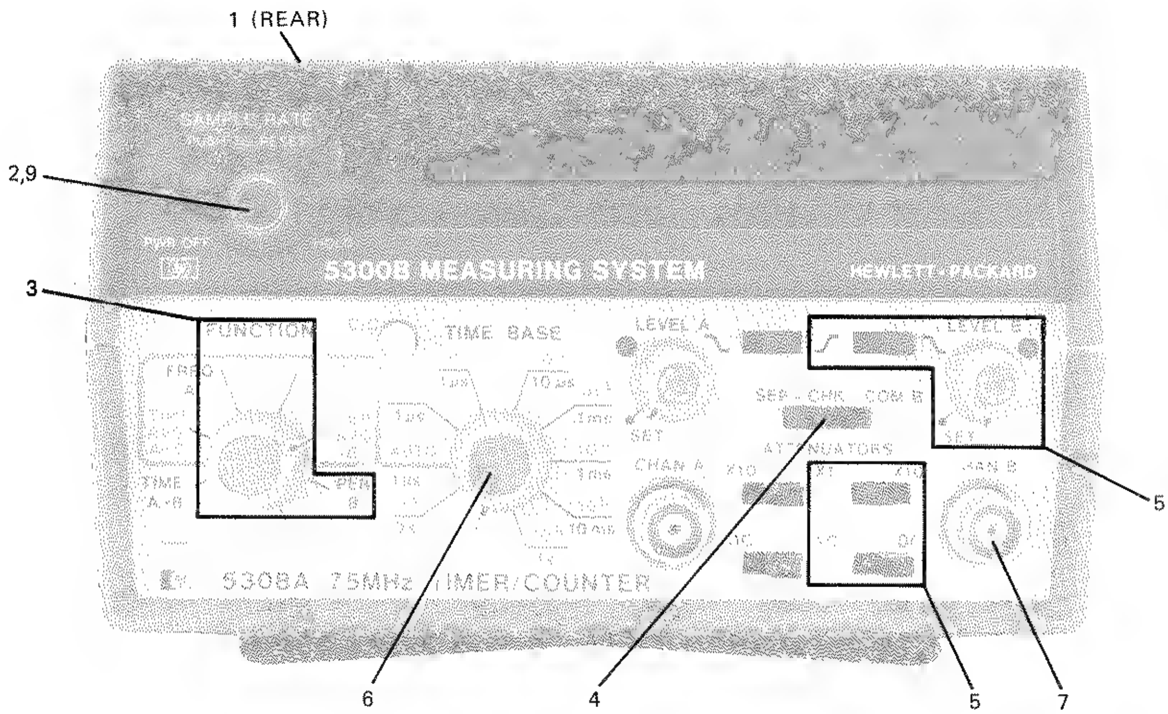
11. Set ATTENUATORS (Channel B) to X10; AC-DC (Channel B) to AC and Channel A slope switch to polarity desired. Set LEVEL A to SET.

NOTE

Ensure that the 'SET' TRIG LEVELS switch on the rear panel is in the .0V position when the LEVEL control is in the SET position.

12. Connect input signal (up to 75 MHz) to be measured to CHAN B connector.
13. Observe display. If display is not stable, rotate LEVEL A control until trigger light illuminates. If necessary, set ATTENUATORS switch for Channel A to X1.
14. Set TIME BASE to desired gate time or to AUTO.

Figure 9H-3-5. Making Channel A and Channel B Frequency Measurements



SEE WARNING ON NEXT PAGE

1. Connect ac power to 5300B ac receptacle.
2. Turn ac power on with 5300B SAMPLE RATE control.
3. Set FUNCTION switch to PER B.
4. Set SEP-CHK-COM B to SEP.

NOTE

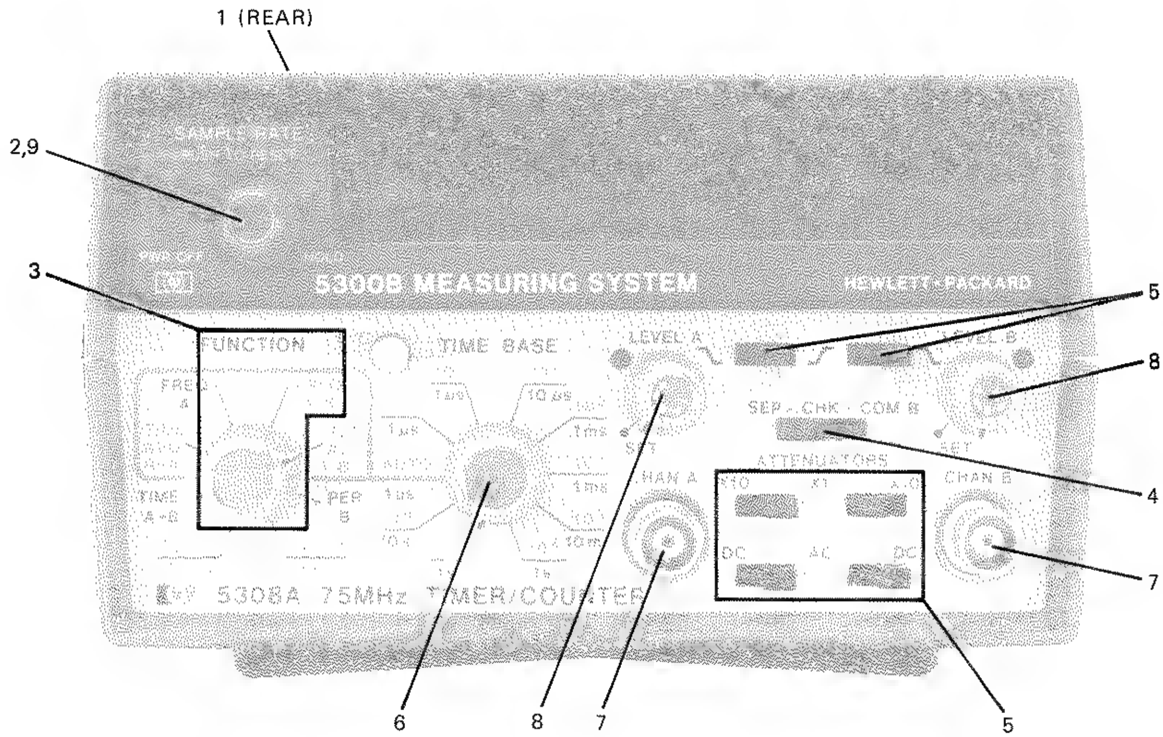
Ensure that the 'SET' TRIG LEVELS switch on the rear panel is in the .0V position when the LEVEL control is in the SET position.

5. Set LEVEL B to SET. Set ATTENUATORS to X10; AC-DC to AC and slope switch to polarity desired.
6. Set TIME BASE to desired resolution or to AUTO.
7. Connect input signal (0 to 5 MHz) to CHAN B connector.
8. Observe display. If display is not stable, rotate LEVEL B control until trigger light illuminates. If necessary, set ATTENUATORS switch for Channel B to X1.
9. Adjust SAMPLE RATE for desired display time.

NOTE

For greater resolution of period measurements, refer to Figure 9H-3-8 for period average measurements.

Figure 9H-3-6. Making Period Measurements

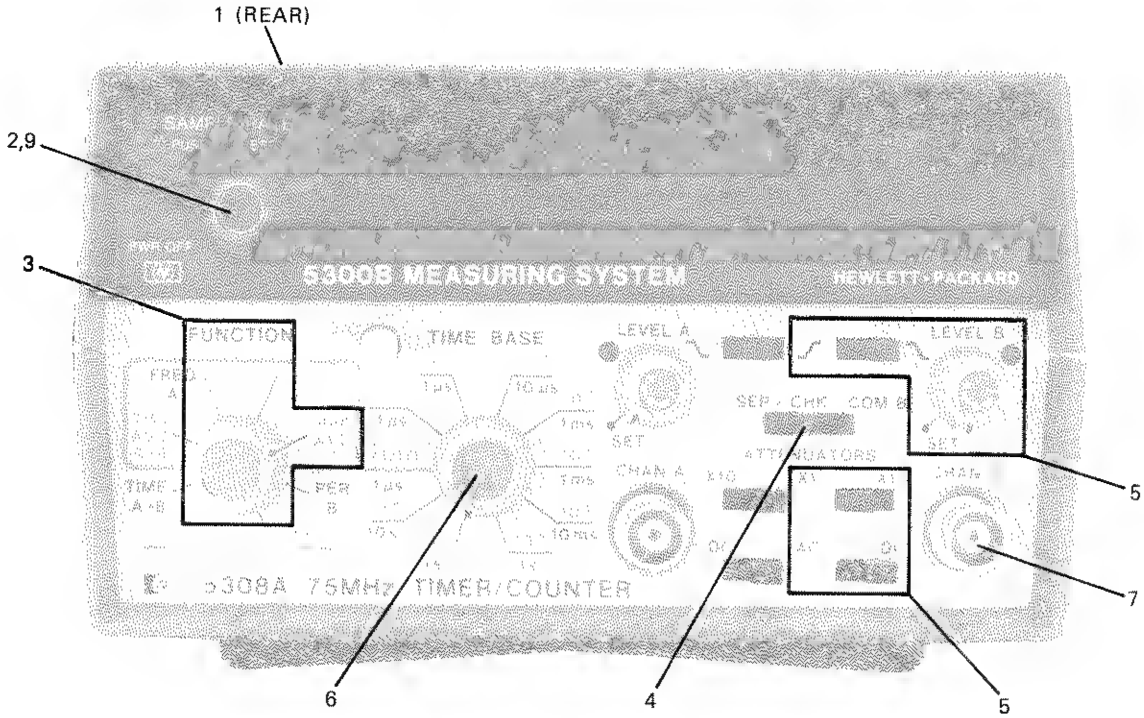


1. Connect ac power to 5300B ac receptacle.
2. Turn ac power on with 5300B SAMPLE RATE control.
3. Set FUNCTION switch to FREQ A/B.
4. Set SEP-CHK-COM B to SEP.
5. Set ATTENUATORS to X1; AC-DC and slope switch as desired.
6. Set TIME BASE to desired setting (1 to 10^8) or AUTO.
7. Connect lower frequency signal (0 to 5 MHz) to CHAN B connector; connect higher frequency signal (0 to 75 MHz) to CHAN A connector.
8. Set the LEVEL A and LEVEL B controls to the middle of the range in which the trigger light illuminates. If necessary, set ATTENUATORS switches to X1.
9. Adjust SAMPLE RATE control for desired display time.

WARNING

TO AVOID POSSIBILITY OF BODILY INJURY AND/OR EQUIPMENT DAMAGE, BE SURE TO OBSERVE POLARITY REQUIREMENTS WHEN CONNECTING TEST LEADS. (HEWLETT-PACKARD RECOMMENDS USING AN ISOLATION TRANSFORMER WHEN MEASURING AC LINE FREQUENCIES.) ADDITIONALLY, DO NOT EXCEED THE INPUT VOLTAGE LIMITATIONS AS SPECIFIED IN TABLE 9H-1-1.

Figure 9H-3-7. Making Ratio Measurements



SEE WARNING ON PAGE 9H-3-11

1. Connect ac power to 5300B ac receptacle.

2. Turn ac power on with 5300B SAMPLE RATE control.

3. Set FUNCTION to PER AVG B.

4. Set SEP-CHK-COM B to SEP.

NOTE

Ensure that the 'SET' TRIG LEVELS switch on the rear panel is in the .0V position when the LEVEL control is in the SET position.

5. Set LEVEL B to SET. Set ATTENUATORS to X10; AC-DC to AC and slope switch to polarity desired.

NOTE

In the 10^8 position of the TIME BASE switch, the display will be in picoseconds with no annunciator shown.

6. Set TIME BASE to desired resolution or to AUTO.

7. Connect input signal (0 to 5 MHz) to CHAN B connector.

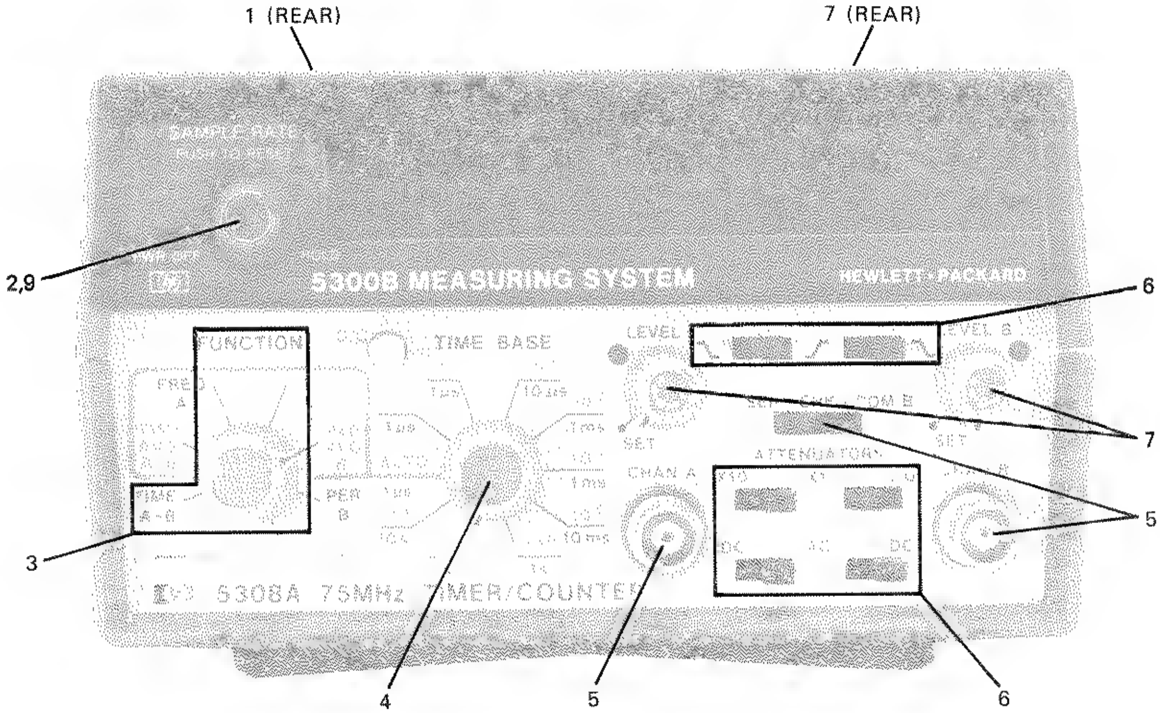
8. Observe display. If display is not stable, rotate LEVEL B control until trigger light illuminates. If necessary, set ATTENUATORS switch for Channel B to X1.

9. Adjust SAMPLE RATE for desired display time.

NOTE

For periods greater than 10 seconds, refer to Figure 9H-3-6 for period measurements.

Figure 9H-3-8. Making Period Average Measurements



SEE WARNING ON PAGE 9H-3-11

1. Connect ac power to 5300B ac receptacle.

2. Turn ac power on with 5300B SAMPLE RATE control.

NOTE

There must be at least 200 ns between the STOP pulse and the next START pulse. When measuring the time interval between the same polarity slope of two pulses from a single source, the PER B mode should be used.

3. Set FUNCTION switch to TIME A→B.

4. Set TIME BASE to desired resolution or to AUTO.

5. If the Start and Stop signals are from separate sources connect the Start signal to CHAN A connector. Connect the Stop signal to CHAN B connector and set the SEP-CHK-COM B to SEP. If the Start and Stop signals are from a common source connect to CHAN B connector and set the SEP-CHK-COM B to COM B.

NOTE

When the SEP-CHK-COM B switch is set to COM B, only the CHAN B ATTENUATORS and AC-DC switches are effective. However, both of the LEVEL controls and slope switches are effective.

6. Set ATTENUATORS to X10; AC-DC switches and slope control switches to settings desired.

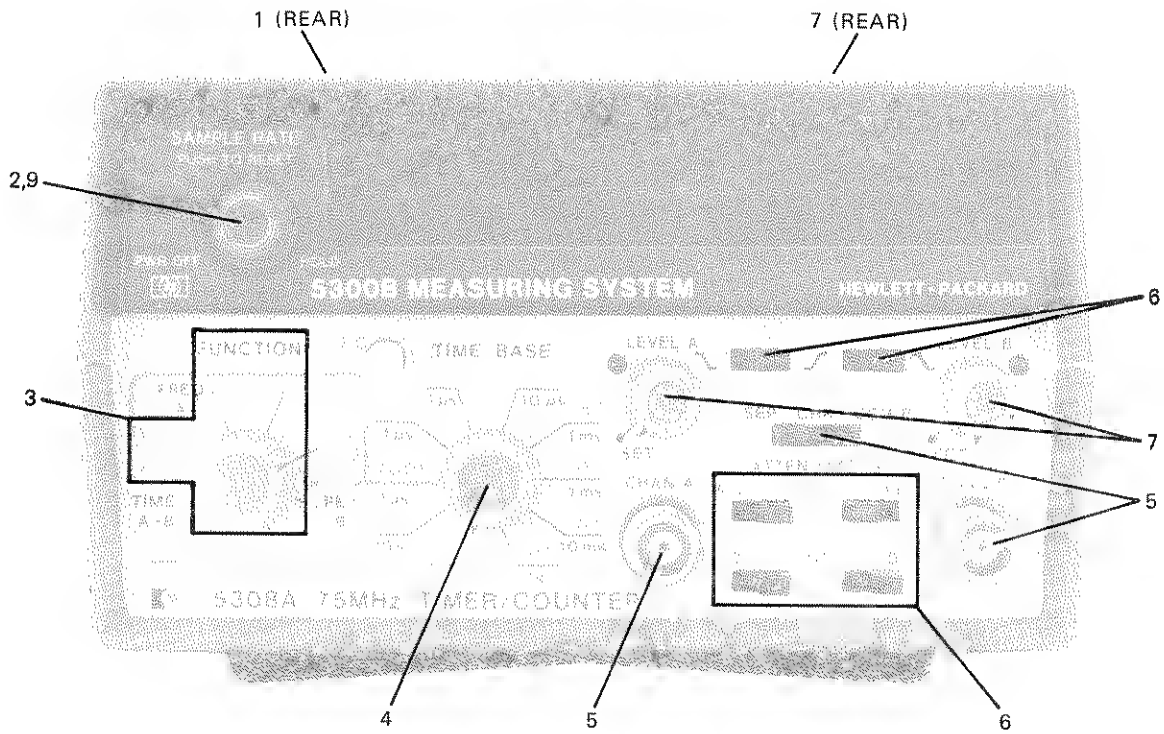
7. If the desired trigger level is not known, set the LEVEL A and LEVEL B controls to the middle of the range in which the trigger light illuminates. If the desired trigger level is known, connect a DVM to the TRIG LEVEL connector for each channel on the rear panel and set the LEVEL A and LEVEL B controls for the desired trigger level. If necessary, set the ATTENUATORS switches to X1.

8. Adjust SAMPLE RATE for desired display time.

NOTE

For greater resolution of time interval measurements refer to Figure 9H-3-10 for time interval average measurements.

Figure 9H-3-9. Making Time Interval Measurements



SEE WARNING ON PAGE 9H-3-11

1. Connect ac power to 5300B ac receptacle.

2. Turn ac power on with 5300B SAMPLE RATE control.

   NOTE

   There must be at least 200 ns between the STOP pulse and the next START pulse. When measuring the time interval average between the same polarity of two pulses from a single source, the PER AVG B mode should be used.

3. Set FUNCTION switch to TIME AVG A→B.

4. Set TIME BASE to desired resolution or to AUTO.

   NOTE

   In the 10^8 position of the TIME BASE switch, the display will be in picoseconds with no annunciator shown.

5. If the Start and Stop signals are from separate sources connect the Start signal to CHAN A connector. Connect the Stop signal to CHAN B connector and set the SEP-CHK-COM B to SEP. If the Start and Stop signals are from a common source connect to CHAN B connector and set the SEP-CHK-COM B to COM B.

   NOTE

   When the SEP-CHK-COM B switch is set to COM B, only the CHAN B ATTENUATORS and AC-DC switches are effective. However, both of the LEVEL controls and slope switches are effective.

6. Set ATTENUATORS to X10; AC-DC switches and slope control switches to settings desired.

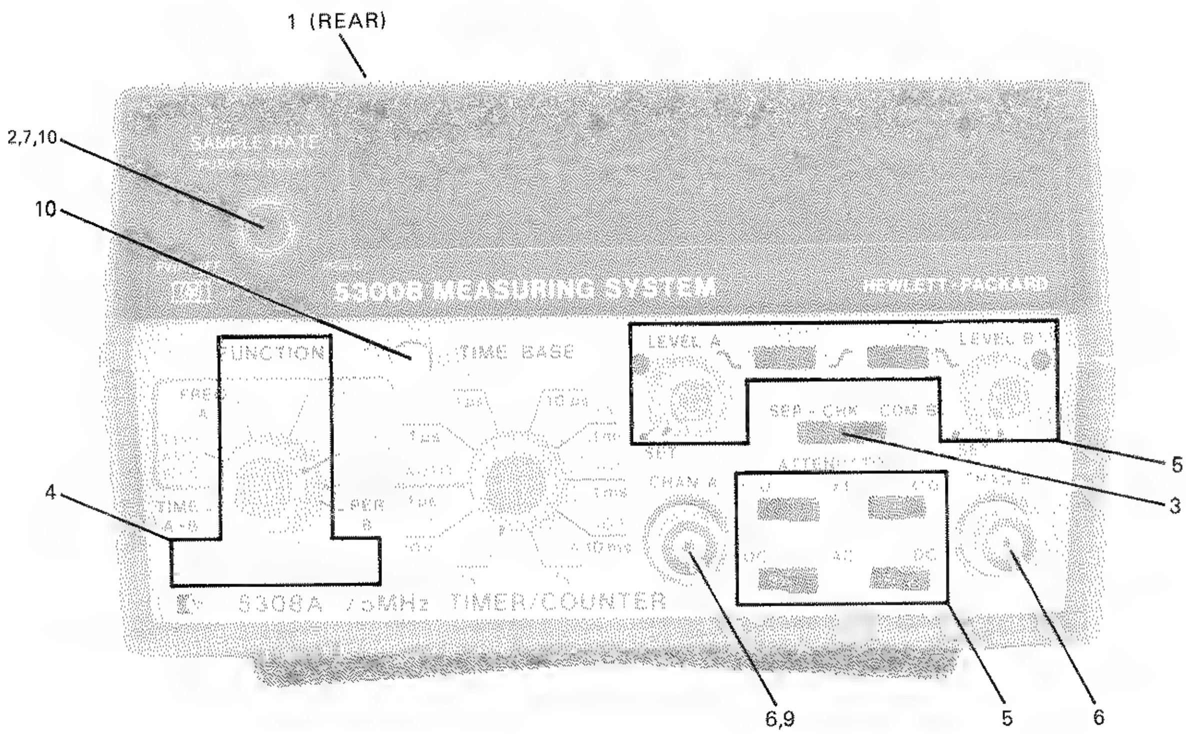
7. If the desired trigger level is not known, set the LEVEL A and LEVEL B controls to the middle of the range in which the trigger light illuminates. If the desired trigger level is known, connect a DVM to the TRIG LEVEL connector for each channel on the rear panel and set the LEVEL A and LEVEL B controls for the desired trigger level. If necessary, set the ATTENUATORS switches to X1.

8. Adjust SAMPLE RATE for desired display time.

   NOTE

   For time intervals in the range of 10 seconds to 10^9 seconds, refer to Figure 9H-3-9 for time interval measurements.

Figure 9H-3-10. Making Time Interval Average Measurements



SEE WARNING ON PAGE 9H-3-11

1. Connect ac power to 5300B ac receptacle.

2. Turn ac power on with 5300B SAMPLE RATE control and adjust SAMPLE RATE for desired display time.

3. Set SEP-CHK-COM B to SEP.

Two-Channel Totalizing

4. To totalize pulses input to Channel A between two pulses input to Channel B, set FUNCTION to TOT A, ⎍⎍ B. To totalize pulses input to Channel A while Channel B is low, set FUNCTION to TOT A, ⎍ B.

NOTE

The position of the Channel B slope switch determines the Channel B trigger level polarity as described in paragraphs 9H-3-36 and 9H-3-37.

5. Set ATTENUATORS to X10; AC-DC switches and slope switches as desired. Set LEVEL A and LEVEL B to SET.

NOTE

Ensure that the 'SET' TRIG LEVELS switch on the rear panel is in the .0V position when the LEVEL control is in the SET position.

6. Connect Channel A input signal to CHAN A connector and Channel B input signal to CHAN B connector.

7. Press RESET. Display will accumulate the number of counts that occur on Channel A per switch settings of step 4. If trigger lights are not illuminated, rotate each LEVEL control until trigger light illuminates. If necessary, set ATTENUATORS switches to X1.

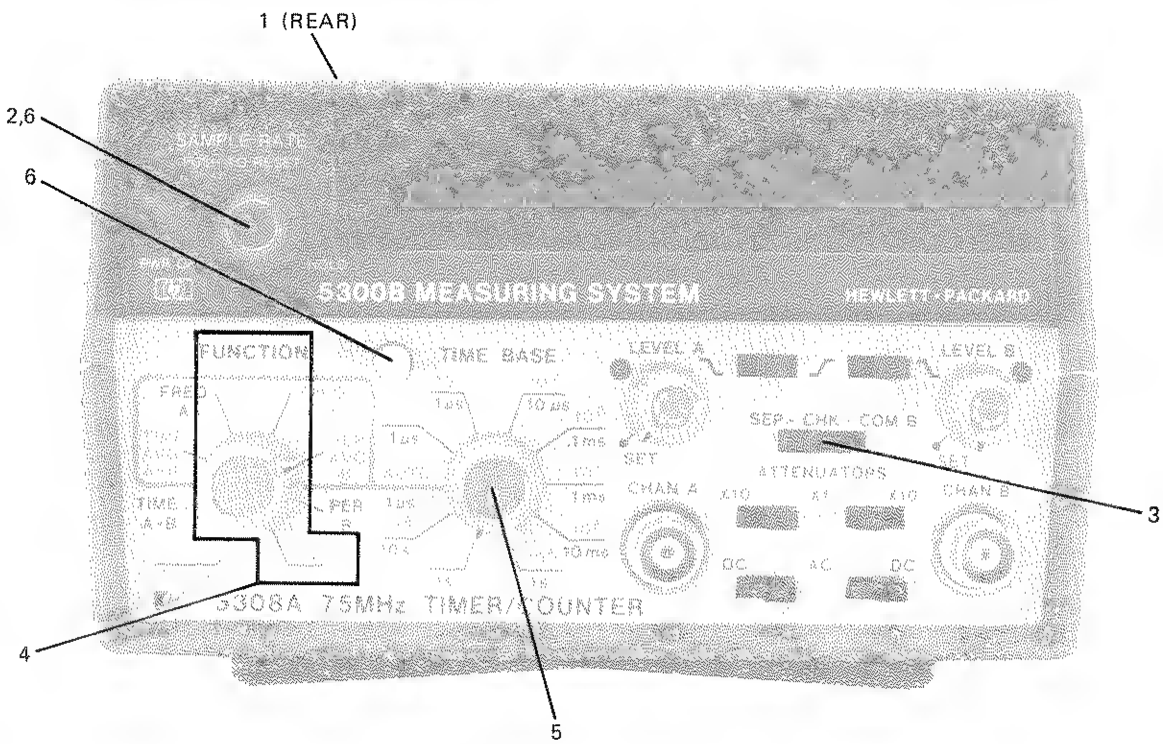
Single-Channel Totalizing

8. To totalize on one channel, perform steps 1, 2, 3 and 5. Set FUNCTION switch to TOT A ⎍⎍ B.

9. Connect input signal to CHAN A connector.

10. Press RESET. Press OPEN/CLOSE switch to initiate totalizing. Display will accumulate at a rate dependent on input signal frequency. When display has accumulated the desired number of counts, press OPEN/CLOSE switch to stop totalizing. If trigger lights are not illuminated, rotate LEVEL A control until trigger light illuminates. If necessary, set ATTENUATORS switch to X1.

Figure 9H-3-11. Making Totalizing Measurements



SEE WARNING ON PAGE 9H-3-11

1. Connect ac power to 5300B ac receptacle.
2. Turn ac power on with 5300B SAMPLE RATE control.
3. Set SEP-CHK-COM B to CHK.
4. Set FUNCTION to TOT A, ⎍⎍ B.
5. Set TIME BASE to desired resolution.

NOTE

Do not connect an input signal to CHAN B during this measurement.

6. Press RESET. Press O/C switch to start, press again to stop stopwatch.
7. Repeat step 6 for each measurement to be taken.

Figure 9H-3-12. Making Stopwatch Measurements

SECTION IX H
5308A 75 MHz TIMER/COUNTER

SUBSECTION IV
THEORY OF OPERATION

9H-4-1. INTRODUCTION

9H-4-2. This section describes the circuit theory of operation for the 5308A. The overall operation of the 5300B in combination with a plug-on module is described in the mainframe portion of the manual.

9H-4-3. CIRCUIT OPERATION

9H-4-4. When plugged onto a 5300B mainframe, the 5308A can measure frequency, frequency ratio, period, period average, time interval and time interval average. Single-channel and two-channel totalize functions are provided. The two-channel function totalizes pulses on Channel A during pulses on Channel B or between pulses on Channel B. Each of these modes of operation is described in the following paragraphs with the aid of a signal flow diagram. The input amplifiers are described first, followed by a description of the ROM circuit that controls the operation and an explanation of the automatic time base mode.

9H-4-5. Input Circuits, Channel A and Channel B

9H-4-6. The input circuits for Channel A are basically identical to those for Channel B (see Figure 9H-4-2) so only the Channel A circuits will be described.

9H-4-7. The Channel A input signal is applied to the front-panel CHAN A connector through AC-DC switch S9 when the switch is in the DC position or through capacitor C6 when the switch is in the AC position. The signal is attenuated by the attenuator circuit R3, R4, C4, C5 when the ATTENUATORS switch is in the X10 position. When the ATTENUATORS switch is in the X1 position the attenuator circuit is bypassed. The signal is connected through SEP-CHK-COM B switch S6, when the switch is in the SEP position, to the Channel A input circuit.

9H-4-8. An overload protection circuit, CR1-CR6 is connected between the Channel A and Channel B inputs. Specifications for the overload protection are listed in Table 9H-1-1. The associated circuitry provides +2.5V and -2.5V for the clipping diodes (CR1, 2, 5 and 6) and for the LEVEL A and LEVEL B controls.

9H-4-9. The input to Channel A is applied to zero-offset buffer Q2A-Q2B. The signal voltage at the gate of Q2A appears at input pin 6 of comparator U2B. Variable resistor R27 provides a balance adjustment to null the offset between the input and output of Q2.

9H-4-10. Comparator U2B compares the output of Q2 with the voltage from the LEVEL A control to provide a digital output (logic 1 or logic 0) to exclusive OR gate U3B. Inductors L1 and L2 and capacitors C9 and C10 connected to U2B form a decoupling circuit to reduce the effects of noise from the 5V power supply. The slope switch for Channel A is connected to pin 5 of U3B. The position of the slope switch determines whether the positive or negative slope of the input waveform will allow gate U3B to be active. The two outputs of U3B are complementary. One of the outputs is applied to U4A, U4B and the other output is applied to U1B, U1D.

9H-4-11. The outputs of gate U3B are converted from ECL levels to TTL levels by U4A, U4B and applied to the remainder of the 5308A circuits which are TTL logic. The outputs of gate U3B are also applied to comparators U1B and U1D which control the illumination of the trigger light indicators.

9H-4-12. Comparators U1B and U1D use positive feedback from the output through capacitor C20 and resistor R58 to the input, to allow the comparators to operate as a one-shot circuit. The diode-capacitor circuit input CR11-C22 or CR12-C29 provides pulse stretching to stretch pulse widths of a few nanoseconds to several microseconds. A single transition of the input signal will cause the LED trigger indicator DS1 to flash momentarily. When the input frequency exceeds approximately 1 kHz, the trigger indicator will remain on. This result occurs because both inputs (pin 4, U1B and pin 10, U1D) are low, both outputs are high, transistor Q8 is turned on and DS1 illuminates.

9H-4-13. ROM (U26) Circuit

9H-4-14. To control the different signal paths for each particular measurement, as shown in Figures 9H-4-2 through 9H-4-8, a system of combinational logic must be used that is based on the function code. In addition, the time base code is used in selecting the decimal point and annunciators (k, μ, Hz, etc.), as well as the measurement's resolution. Because many control lines are needed, the 5308A uses a ROM (read only memory), instead of controlling the logic directly from the front-panel switches. The 16 output lines from the ROM reflect the programmed logic states of a particular address in the ROM. The front-panel switches combine to select the ROM's addresses and, hence, the ROM's output states. In addition to controlling the signal flow logic, the ROM's outputs also drive the annunciator lines through the U10 inverters. The remaining three ROM outputs go

to the 4-to-10 line decoder, U25, where the 3 lines are decoded to drive the decimal point lines.

9H-4-15. When operating in the AUTO mode, the $\overline{\text{AUTO/X1}}$ line from J1 activates the Exponent Counter/Latch, U28. This is a tri-state device that is normally in its high-impedance (off) state; however, in AUTO, the OD (output disable) inputs are Low, and the device is free to count $\overline{\text{LOG}}$ pulses. Since the log pulses occur for each 10^N accumulation of the F2 signal, they directly represent the magnitude of the measurement being made and can, therefore, be used to adjust the decimal point and annunciators as the measurement progresses.

9H-4-16. When a measurement is in progress, the results of the previous measurement are being displayed and the exponent counter is being clocked by $\overline{\text{LOG}}$ pulses. The output states remain fixed, however, to maintain the proper decimal point and annunciator for the current display. Once the measurement ends, both inputs of U19C go Low and allow U28 to transfer its internally stored count to the ROM.

9H-4-17. Automatic Time Base Mode

9H-4-18. When the TIME BASE switch is set to the AUTO position, the counter provides a special measurement feature for four modes of operation: Time Interval Average, Frequency A, Frequency A/B, and Period Average B. For any one of these modes, the counter will perform a measurement within a one second gate time. The gate time is not fixed but for the majority of cases will vary between 0.11 s and 1.1 s.

9H-4-19. The measurement starts when the Auxiliary Gate Flip Flop (AGFF, U17A) is clocked by the "time zero" $\overline{\text{LOG}}$ pulse. When the Q output of U17A goes High, it fires the 0.11 second one-shot, U23. Since the $\overline{\text{AUTO/X1}}$ line from J1 is Low, U24B enables U12E to pass the .11 second pulse to the clock input of U17B. The trailing edge of the pulse clocks U17B, causing the $\overline{Q}$ output to go Low. This enables the next $\overline{\text{LOG}}$ pulse to terminate the measurement by clocking U17A.

9H-4-20. Recall that a $\overline{\text{LOG}}$ pulse occurs for each 10^N event of the F2 signal; however, any $\overline{\text{LOG}}$ pulses that occur prior to setting U17B (a delay of 0.11 seconds) are ignored. The measurement ends with the $\overline{\text{LOG}}$ pulse that occurs immediately after U17B sets. This always corresponds to a gate time between .11 s and 1.1 s, as illustrated in Figure 9H-4-1.

9H-4-21. As an example in explaining the graph in Figure 9H-4-1, assume a period average measurement is being made with an input frequency of 400 Hz. One period of 400 Hz is 1/400 = .0025 s = 2.5 ms. Since 10 periods must be counted to produce the first log pulse, this pulse would occur after 25 ms (2.5 ms ÷ 10). This log pulse is ignored, since it falls within the 110 ms (.11 s) delay of the one-shot. The next log pulse occurs 10 times later at 250 ms (25 ms ÷ 10). This pulse ends the measurement since the .11 s inhibit time has elapsed. The gate time, then, is .25 s.

9H-4-22. Frequency A Mode

9H-4-23. In the frequency mode, the Channel A signal is sent from U4(4) to the F1 switch (see Frequency Mode Flow Diagram, Figure 9H-4-2). Gates U5E and U5D couple the signal to U8B(3) where it is gated to the counting decades by the Auxiliary Gate FF, U17A.

9H-4-24. Prior to making a measurement, the $\overline{\text{INHIBIT}}$ line resets U17A and B. The resultant Low on the Q output of U17A prevents the Auxiliary Main Gate from passing the Channel A signal to the counting decades. At the end of the sample rate rundown, the $\overline{\text{INHIBIT}}$ line returns High, followed by a $\overline{\text{LOG}}$ pulse. Gates U7E, U7D, and U20B couple this pulse to the clock input of U17A. Clocking U17A transfers the High on the D input to the Q output where it opens the Auxiliary Main Gate at U8B(2). It also enables U12A and D and places a Low on the clock input of U17B.

9H-4-25. The Channel A signal passes through the High Speed Decade, U13 and 18, before entering the mainframe on the F1 line. As the mainframe begins accumulating F1 counts, the mainframe's Time Base Decades also begin accumulating 10 MHz clock pulses via U21A and D. Once the Time Base Decades reach a count equal to the selected gate time, a pulse is generated on the $\overline{\text{TB OUT}}$ line that toggles U17B via Q8, U16C, U12A and D. The following $\overline{\text{LOG}}$ pulse is sent through Q5, U24A, U7E and D, and U20B to close the Auxiliary Gate FF, thereby closing the Auxiliary Main Gate.

9H-4-26. Frequency A/B Mode

9H-4-27. The frequency A/B mode performs a ratio measurement between the Channel A and Channel B frequencies. This mode is similar to the FREQ A mode, since a frequency measurement is simply a ratio between the Channel A frequency and the 10 MHz internal clock. Instead of sending the 10 MHz clock to the Time Base Decade, the counter substitutes the Channel B signal. Refer to the Frequency A/B Mode Flow Diagram, Figure 9H-4-3.

9H-4-28. At the beginning of the measurement, the "time zero" $\overline{\text{LOG}}$ pulse clocks the AGFF(U17A) via U7E, U7D, and U20B. The resultant High on the Q output opens the Auxiliary Main Gate at U8D and allows the Channel A signal from U4A to pass through U5E and D and U8B and D. From there, it passes through the High Speed Decade and into the mainframe's counter assembly via the F1 line. At the same time, the Channel B signal enters the mainframe's Time Base Decade through U21E and U21D.

9H-4-29. When the AGFF was set with the "time zero" $\overline{\text{LOG}}$ pulse, it enabled U12A and U12D and placed a Low on the clock input of U17B. Once the Time Base Decades reach a count equal to the selected gate time, a pulse is

Hz	GATE TIME
10	1 s
9	1.1 s
8	1.25 s
7	1.43 s
6	1.66 s
5	2.0 s
4	2.5 s
3	3.33 s
2	5.0 s
1	10 s

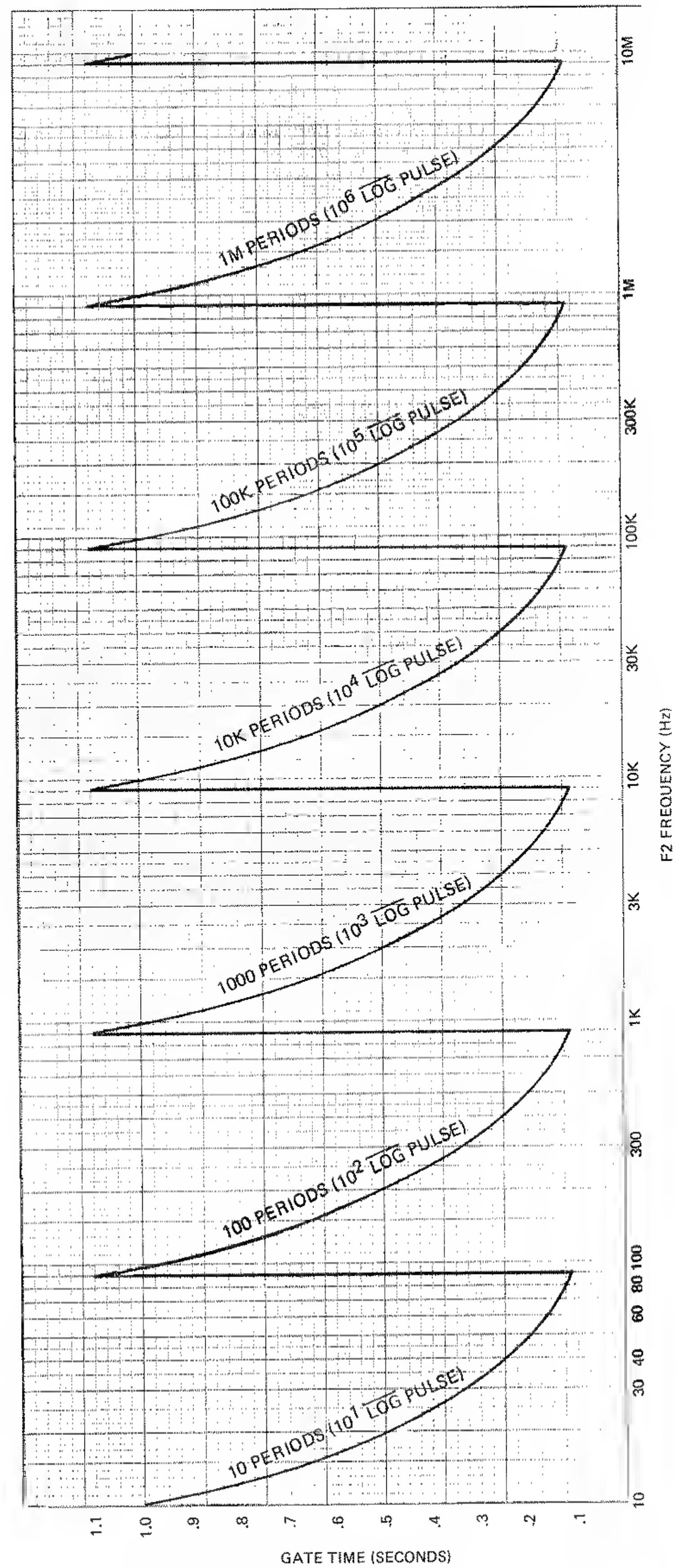


Figure 9H-4-1. Gate Time Versus F2 Frequency

generated on the $\overline{\text{TB OUT}}$ line that clocks U17B by disabling U12A. The next $\overline{\text{LOG}}$ pulse, which follows immediately thereafter, passes through Q7, U24A, U7E and D, and U20B and closes the AGFF. The Low output of U17A(5) disables U8B and ends the measurement.

9H-4-30. Period B Mode

9H-4-31. In a single period measurement, the internal clock signal is counted in the mainframe's counter assembly during one period of the Channel B signal. Before the clock signal is counted, it is first divided in the Time Base Decades (mainframe). The division is a function of the front-panel Time Base switch and serves to vary the measurement's resolution. Refer to Period B Mode Flow Diagram, Figure 9H-4-4.

9H-4-32. At the beginning of the measured period, the output of U4C goes Low and clocks the AGFF, U17A, via U7C, U7D, and U20B. The resultant High on the Q output enables the $\overline{\text{TB OUT}}$ signal to pass through the Auxiliary Main Gate, and into the High Speed Decade. The signal then travels to the mainframe's counter on the F1 line.

9H-4-33. When the AGFF was set at the beginning of the period, the $\overline{Q}$ output went Low and caused U12B and D to clock U17B. This occurs almost instantly after the AGFF sets and lags only by the propagation delays of the gates themselves. Once clocked, U17B places a Low on the D input of U17A. Thus, the AGFF is ready to close the Auxiliary Main Gate at the end of the period, i.e., the next negative-going output of U4C.

9H-4-34. Period Average B Mode

9H-4-35. In a period average measurement, the counter samples a group of periods and displays the average value. The numher of periods selected is always in powers of ten (10^2, 10^3, 10^4, etc.) and is a function of the TIME BASE switcb. For the following description, refer to Period Average B Flow Diagram, Figure 9H-4-5.

9H-4-36. At the beginning of the measurement, the "time zero" $\overline{\text{LOG}}$ pulse clocks the AGFF(U17A) via U7E, U7D, and U20B. This opens the Auxiliary Main Gate at U8B and allows the 10 MHz clock signal to enter the High Speed Decade and the mainframe's counter assembly. At the same time, the Channel B signal is sent to the mainframe's Time Base Decade through U21E and D.

9H-4-37. In addition to opening the Auxiliary Main Gate, the High level at U17A(5) also enables U12A. This places a low on the clock input of U17B. Once the mainframe's Time Base Decade accumulates 10^N periods, the $\overline{\text{TB OUT}}$ line goes Low, which disables U12A and U12D and clocks U17B. This places a Low on the D input of U17A, allowing the next $\overline{\text{LOG}}$ pulse (immediately following) to clock U17A and close the Auxiliary Main Gate.

9H-4-38. Totalize A ⊓⊓ B Mode

9H-4-39. This mode allows Channel A pulses to totalize for the time hetween Channel B pulses. The counter can be used as a stop watch when in the CHK function by using the O/C switch to manually start and stop the accumulation of clock pulses. Both modes are explained in the following paragraphs. Refer to the Totalize A ⊓⊓ B Mode Flow Diagram, Figure 9H-4-6.

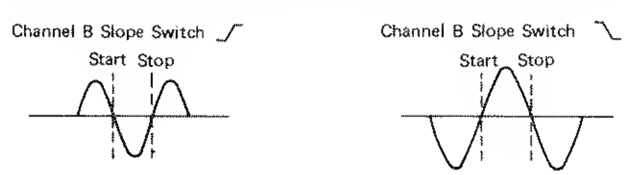
9H-4-40. TOTALIZE "A" BETWEEN "B" PULSES. Assume that Channel B is set to trigger on the positive slope. See Totalize A ⊓⊓ B Flow Diagram, Figure 9H-4-6. The first positive-going Channel B pulse forces U7C(4) Low and clocks U17A through U7D and U20B.

9H-4-41. The Channel A signal passes through U21C and D and enters the mainframe's Time Base Decades. The signal is divided by a factor determined by the setting of the TIME BASE switch. As the divided signal returns on the $\overline{\text{TB OUT}}$ line, it passes through Q8, U5B and D, U8B and D, and the High Speed Decade and returns to the mainframe on the F1 line. Immediately after the AGFF was set, the Low output of $\overline{Q}$ disabled U12B and U12D. This caused U17B to clock a Low level onto its $\overline{Q}$ output. Upon arrival of the next positive-going Channel B pulse, the AGFF is clocked in the same manner as before. This time, however, the flip-flop transfers a Low level to the Q output, which disables U8B and terminates the measurement. No further measurements can he taken until the RESET button is pushed. This releases the $\overline{\text{INHIBIT}}$ signal from the reset inputs of U17A and B.

9H-4-42. TOTALIZE WITH O/C SWITCH. This mode operates in the same manner as that described above, except that the Channel B pulses are manually produced with the O/C switch. Pushing the O/C switch grounds U16A(1), causing a High level at pin 2. The two cross-coupled inverters prevent contact bounce of the O/C switch from disrupting the other circuits. The differentiator circuit of C16 and R33 produces a positive spike from the voltage level change at U16 pin 2. This spike passes through U20A to pin 4 of U20B. Since this is an exclusive OR gate, the two positive inputs force the output to a Low state. On the trailing edge of the spike, the output of U20B returns High and clocks the AGFF.

9H-4-43. Totalize A ⊔ B

9H-4-44. This mode operates in the same manner as does the Totalize A ⊓⊓ B Mode shown in Figure 9H-4-6 except the counter totalizes Channel A pulses while Channel B is held at a specified level. The difference between the modes results from a static level change at U11A(13). In this mode, the level is Low. Input triggering is related to the slope switch setting as follows:



9H-4-45. Referring again to Figure 9H-4-6, assume that U7D pin 8 is High. After reset and before the first Channel B input pulse, the initial conditions are as follows: U11A(12) is High, since both inputs are Low; U20B(6) is Low, since both inputs are High. When the input signal goes Low, U7C(4) goes High, U7D(8) goes Low, U20B(6) goes High and clocks the AGFF. When the flip-flop toggles, it removes the Low on U11A(1,2) and results in a Low on U20B(4). Since both inputs are Low, tbe output of U20B also goes Low. This enables U20B to respond to the stop portion of the input pulse. When the input signal returns High, U7D(8) returns High and U20B clocks the AGFF close, ending the measurement.

9H-4-46. TIME INTERVAL AVERAGE A TO B MODE

9H-4-47. Tbe number of time intervals to be averaged is determined by the TIME BASE switch setting, e.g., 10^3, 10^4, 10^5, etc. time intervals. During each time interval, tbe mainframe's Time Base Decades record the number of time intervals by counting syncbronized Channel A pulses. When the counter accumulates the proper number of intervals, it terminates the measurement with a $\overline{\text{LOG}}$ pulse. Refer to the Time Interval Average Flow Diagram, Figure 9H-4-7 for the following descriptions.

9H-4-48. The "time zero" $\overline{\text{LOG}}$ pulse enables the counter to make a measurement by clocking the AGFF (U17A). This places a High on U8B(2) and allows the gate to pass clock pulses during each individual time interval. After the Channel A pulse sets flip-flop U6C and D, the next 10 MHz clock pulse sets U9B, which enables U14A to pass the 10 MHz clock signal. The signal accumulates counts in the High Speed Decade and in the mainframe's counter until the Channel B pulse ends the time interval. It does this by setting U6A and B, allowing the next clock pulse to set U9A. The High on the Q output disables U14A from passing tbe clock pulses.

9H-4-49. The counter continues accumulating clock pulses during the time A to B until 10^N time intervals have been measured. At this point, the $\overline{\text{TB OUT}}$ line goes Low and clocks U17B via Q6, U16C, U12A, and U12D. When U17B sets, it places a low level on the D input of U17A. The following $\overline{\text{LOG}}$ pulse clocks U17A. This ends the measurement by disabling U8B.

9H-4-50. TIME INTERVAL A TO B MODE

9H-4-51. A single time interval is measured by opening the gate with the Channel A signal and counting the 10 MHz clock signal (or 10 MHz/ 10^N) until the Channel B signal closes the gate. Refer to Time A → B Mode Flow Diagram, Figure 9H-4-8.

9H-4-52. When Channel A triggers, it sends a positive pulse to differentiator C30 and R63. The resulting spike sets flip-flop U6C and D and places a High on U9B(12). On the next positive-going edge of the clock signal, the $\overline{Q}$ output goes Low and enables U14C.

9H-4-53. Prior to the Channel A trigger pulse, U20B pin 4 was High, due to the inputs of U11A being Low; and U20B(5) was High, since U7A(1) was Low. These conditions caused U20B(6) to sit at a Low level. Once U14C(8) goes High, it removes the High level at U7D(8) and allows U20B to clock the AGFF. The resultant High on the Q output causes U20B pins 4 and 6 to go Low. U8B and D pass the divided clock signal to the High Speed Decade and then to the mainframe. The Low on U17A(6) is inverted by U12C and U12D to clock U17B. The resultant Low on $\overline{Q}$ enables U17A to close at a later time.

9H-4-54. Once the Channel B pulse arrives, it sets flip-flop U6A and B, causing a High on the D input of U9A. The next clock pulse disables U14C by placing a Higb on pins 9 and 10. This disables U14C and allows U7D(8) to go High and close the AGFF through U20B. The Low on the $\overline{Q}$ output of U9A enables U14B to pass the 10 MHz clock to the reset lines of U9A and B.